Euro-Par 2015 Vienna

21st International
European Conference on
Parallel and Distributed Computing

http://www.europar2015.org

Conference and Workshop Program



Vienna, Austria, 24-28 August 2015

Parallel Computing

TU WIEN

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FÜR !NFORMATIK

Faculty of Informatics

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Editorial Office | Contact:
Alexandra Carpen-Amarie
Sascha Hunold
Research Group for Parallel Computing
Faculty of Informatics | Institute of Information Systems
europar2015@par.tuwien.ac.at
http://www.europar2015.org

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Preface

Dear Friends and Colleagues, dear all Euro-Par 2015 Participants,

Welcome to the 21st edition of Euro-Par, the prime international conference on all aspects of parallel and distributed processing on European ground, this time taking place in Vienna, Austria, hosted by the Parallel Computing group of the Vienna University of Technology (TU Wien). The next days will bring us a hopefully lively, interesting, and stimulating workshop and conference program with plenty of opportunity for discussion and interaction. For the conference, 51 papers will be presented in parallel sessions following the traditional Euro-Par organization into topics, of which there were this year 13 in all (for one topic, no papers will be presented). Two papers were selected as distinguished papers, and will be presented in plenary sessions. Also in plenary sessions are three technical keynote talks which should be of considerable interest to everybody in our field. Finally, the panel on the future of parallel, distributed, and high-performance computing in Europe will be an opportunity to take stock of our field, from a European perspective, and you are all invited to join the discussion. This year there are 12 Euro-Par workshops taking place on Monday and Tuesday. We will spend some free and hopefully pleasant time together at the conference reception on Tuesday evening in the Vienna City Hall (Wiener Rathaus), and on Thursday evening at the Schottenheuriger. We look forward to and wish all of you interesting and well-spent days in Vienna!

The relevance of Euro-Par is first and foremost due to the researchers who chose Euro-Par as the venue for presentation of results. We therefore warmly thank all contributors to submitted papers, and hope that the feedback, whether the contribution was accepted or not, merit the effort. Second, the conference lives from all who attend and wish to engage in discussion with presenters and other attendees, and we thank everybody who is here now for the next couple of days. We hope it will have been worthwhile.

Preface

A few sponsors contributed to make the conference financially feasible, and we therefore thank Google, h.o.-COMPUTER, Vienna Convention Bureau, Stadt Wien, and Springer for their commitment. Needless to say, sponsors have no influence on the content of the conference and were not involved in the planning at any stage.

The following few pages contain the full conference and workshop program, and a few remarks on practical matters and on the social events. Do not hesitate to get in touch with either of us of the organizational team for any matters that may come up.

We wish you a good conference and a wonderful stay in Vienna.

Vienna, August 2015

Jesper Larsson Träff
Sascha Hunold
Francesco Versaci
Alexandra Carpen-Amarie
Christine Kamper
Margret Steinbuch

Table of Contents

Preface 1

Venue 5

Organization 7

Conference and Program Committees 7
Steering Committee 10

Keynotes 11

Keynote 1 11
Keynote 2 12
Keynote 3 14

Panel 15

Conference Program 16

Overview 16
Day 1 - Wednesday, Aug 26, 2015 18
Day 2 - Thursday, Aug 27, 2015 21
Day 3 - Friday, Aug 28, 2015 22

Workshops 23

Overview 23

Workshops Program Monday, Aug 24 25

BigDataCloud - Big Data Management in Clouds 25
Euro-EDUPAR - Parallel and Distributed Computing Education for Undergraduate Students 25
LSDVE - Large Scale Distributed Virtual Environments 27
OMHI - On-chip Memory Hierarchies and Interconnects: organization, management and implementation 27
PADABS - Parallel and Distributed Agent-Based Simulations 28
Resilience - Resiliency in High Performance Computing with Clouds, Grids, and Clusters 29

Table of Contents

Workshops Program Tuesday, Aug 25 31

HeteroPar - Algorithms, Models, and Tools for Parallel Computing on Heterogeneous Platforms 31

PELGA - Performance Engineering for Large-scale Graph Analytics 32

REPPAR - Reproducibility in Parallel Computing 33

ROME - Runtime and Operating Systems for the Many-core Era 34

UCHPC - UnConventional High Performance Computing 34

VHPC - Virtualization in High-Performance Cloud Computing 35

Social Events 36

Welcome Reception 36

Conference Banquet 36

Venue

Venue Address

The conference takes place at the Vienna University of Technology, Austria.
The conference venue is the Faculty of Electrical Engineering and Information Technology, which is located at Gußhausstraße 27-29, 1040 Wien.
The workshops, however, will take place in Gußhausstraße 25, 1040 Wien, which is only one building away (it is part of the dark green block of buildings, see map below).

The venue (dark green building on map) is located near the subway station Karlsplatz, where three subway lines stop (U1/U2/U4).

Take either exit Resselpark or Karlsplatz and you will be in front of the main building of the Vienna University of Technology. Go to the fountain (in front of the Karlskirche / St. Charles Church) and turn right into Karlsgasse. Follow this street which will bring you directly to the conference venue.

Venue

Registration desk

The registration desk for workshop and conference participants will be located at the conference venue in Gußhausstraße 27-29, 1040 Wien. The registration desk will be open every day from 8:00.

Getting Around in Vienna

In case you have or find time to explore Vienna before, after, or during Euro-Par 2015, doing so by foot or by public transportation is by far the best and easiest way. The historic inner city is 5-10 minutes walking distance from TU Wien at Gusshausstrasse, via Karlsplatz and the State Opera.

There are a number of subways from Karlsplatz (U1, U2, U4) from which you can reach most of Vienna very easily and within a few minutes. There are also a number of tramlines at Wiedner Haupstrasse and from Karlsplatz that can be very convenient (1, 62, Badner Bahn). Buses in Vienna are also useful. A single adult fare costs 2.20 Euros, and there are various day passes which make sense in case you want to get around. Tickets for the subway have to be bought in advance (there a machines at all stations), tram and bus tickets can be bought in advance or in the car. A ticket is valid for all means of public transportation within a zone.

To get to and from the airport, we recommend the public airport bus from Schwedenplatz (8 Euros single fare), the S-Bahn S7 from "Wien Mitte" (4.40 Euros single fare), or the City Airport Train (CAT, 11 Euros single fare) also from "Wien Mitte". There are several shuttle services, and taxis with fixed prices for the airport.

Badges

Please wear/bring your conference badge during the conference and social events to help us with the organizational matters.

Organization

Conference and Program Committees

Conference Committee

General Chair

Jesper Larsson Träff	Vienna University of Technology, Austria

Proceedings Chair

Francesco Versaci	Vienna University of Technology, Austria

Workshop Co-Chair

Sascha Hunold	Vienna University of Technology, Austria

Local organization

Christine Kamper	Vienna University of Technology, Austria
Margret Steinbuch	Vienna University of Technology, Austria
Alexandra Carpen-Amarie	Vienna University of Technology, Austria

Program Committee

Topic 1: Support Tools and Environments

Rosa Badia	Barcelona Supercomputing Center, Spain
Karl Fürlinger	LMU Munich, Germany
Todd Gamblin	Lawrence Livermore National Laboratory, USA
Nathan R. Tallent	Pacific Northwest National Laboratory, USA
Marios D. Dikaiakos	University of Cyprus, Cyprus
Brian Wylie	Forschungszentrum Juelich, Germany
Thilo Kielmann	Vrije Universiteit Amsterdam, The Netherlands
Matthias S. Mueller	RWTH Aachen, Germany

Topic 2: Performance Modeling, Prediction and Evaluation

Felix Wolf	Technische Universität Darmstadt, Germany
Marian Vajteršic	University of Salzburg, Austria
Laura Carrington	San Diego Supercomputer Center, USA
Frédéric Suter	IN2P3 Computing Center, France
Miquel Pericàs	Chalmers University of Technology, Sweden

Topic 3: Scheduling and Load Balancing

Denis Trystram	Grenoble Institute of Technology, France
Hans Kellerer	Graz University of Technology, Austria
Henri Casanova	University of Hawai`i, USA
Vitus Leung	Sandia National Laboratories, USA
Giorgio Lucarelli	LIG Grenoble, France

Organization

Program Committee

Ariel Oleksiak	Poznan Supercomputing Center, Poland
Natasha Shakhlevich	University of Leeds, UK
Leonel Sousa	University of Lisbon, Portugal

Topic 4: Architecture and Compilers

Franz Franchetti	Carnegie Mellon University, USA
Jens Knoop	Vienna University of Technology, Austria
Markus Schordan	Lawrence Livermore National Laboratory, USA
Louis-Noël Pouchet	University of California, Los Angeles, USA
Sid Touati	INRIA, France

Topic 5: Parallel and Distributed Data Management

André Brinkmann	University of Mainz, Germany
Harald Kosch	University of Passau, Germany
Gabriel Antoniu	INRIA Rennes, France
Veronika Sonigo	FEMTO-ST, Besançon, France

Topic 6: Grid, Cluster and Cloud Computing

Frédéric Desprez	INRIA, France
Radu Prodan	University of Innsbruck, Austria
Adrien Lebre	INRIA, France
Helge Meinhard	CERN, Switzerland
Rizos Sakellariou	University of Manchester, United Kingdom
Uwe Schwiegelshohn	TU Dortmund University, Germany
Domenico Talia	University of Calabria, Italy
Ramin Yahyapour	Georg-August University of Göttingen, Germany

Topic 7: Distributed Systems and Algorithms

André Schiper	EPFL, Switzerland
Josef Widder	Vienna University of Technology, Austria
Antonio Casimiro	University of Lisbon, Portugal
Christof Fetzer	Dresden University of Technology, Germany
Marta Patino-Martinez	Technical University of Madrid, Spain
Pierre Sens	LIP6/INRIA Paris Rocquencourt, France

Topic 8: Parallel and Distributed Programming, Interfaces and Languages

Bill Gropp	University of Illinois at Urbana-Champaign, USA
Erwin Laure	KTH Royal Institute of Technology, Sweden
Keshav Pingali	The University of Texas at Austin, USA
Rajeev Thakur	Argonne National Laboratory, USA
Michael Gerndt	Technische Universität München (TUM), Germany

Organization

Program Committee

Topic 9: Multi- and Many-core Programming

Marco Aldinucci	University of Torino, Italy
Siegfried Benkner	University of Vienna, Austria
Hans Vandierendonck	Queen's University Belfast, UK
Franscisco De Sande	Universidad de La Laguna, Spain
Antoniu Pop	University of Manchester, UK
Massimo Torquati	University of Pisa, Italy
Samuel Thibault	INRIA Bordeaux, France
Massimiliano Meneghin	Autodesk Research, Toronto, Canada
José Daniel García	Charles III University of Madrid, Spain

Topic 10: Theory and Algorithms for Parallel Computation

Peter Sanders	Karlsruhe Institute of Technology, Germany
Robert Elsässer	University of Salzburg, Austria
Leah Epstein	University of Haifa, Israel
Pierre Fraigniaud	Paris Diderot University - Paris 7, France
Geppino Pucci	University of Padua, Italy

Topic 11: Communication, Routing and Networks

Torsten Hoefler	ETH Zurich, Switzerland
Holger Fröning	Heidelberg University, Germany
Mondrian Nüssle	Extoll GmbH, Germany
Federico Silla	Technical University of Valencia, Spain
Mitch Gusat	IBM Zurich, Switzerland
Tor Skeie	University of Oslo, Norway

Topic 12: Numerical Methods and Applications

Paolo Bientinesi	RWTH Aachen, Germany
Wilfried Gansterer	University of Vienna, Austria
Daniel Ruprecht	Università della Svizzera italiana, Lugano, Switzerland
Xavier Vasseur	CERFACS, France

Topic 13: Accelerator Computing

Jörg Keller	University of Hagen, Germany
Andreas Steininger	Vienna University of Technology, Austria
Lee Howes	Qualcomm, USA
Michael Klemm	Intel, Deutschland
Naoya Maruyama	RIKEN, Japan
Norbert Eicker	Jülich Supercomputing Centre, Germany
Erik Saule	UNC Charlotte, USA
Benedict Gaster	University of the West of England, UK

Organization

Program and Steering Committees

Steering Committee

Chair

Christian Lengauer	University of Passau, Germany

Vice-Chair and Workshop Co-Chair

Luc Bougé	ENS Rennes, France

European Representatives

Marco Danelutto	University of Pisa, Italy
Emmanuel Jeannot	LaBRI-INRIA, Bordeaux, France
Christos Kaklamanis	Computer Technology Institute, Greece
Paul Kelly	Imperial College, UK
Thomas Ludwig	University of Hamburg, Germany
Emilio Luque	Autonomous University of Barcelona, Spain
Tomàs Margalef	Autonomous University of Barcelona, Spain
Wolfgang Nagel	Dresden University of Technology, Germany
Rizos Sakellariou	University of Manchester, UK
Fernando Silva	University of Porto, Portugal
Henk Sips	Delft University of Technology, The Netherlands
Domenico Talia	University of Calabria, Italy
Felix Wolf	Technische Universität Darmstadt, Germany

Honorary Members

Ron Perrott	Oxford e-Research Centre, United Kingdom
Karl Dieter Reinartz	University of Erlangen-Nuremberg, Germany

Observers

Jesper Larsson Träff	Vienna University of Technology, Austria
Denis Trystram	Grenoble Institute of Technology, France

Keynotes

Keynote 1

Michel Raynal
IRISA, University of Rennes, France

Concurrent Systems: Hybrid Object Implementations and Abortable Objects

Wednesday, Aug 26, 2015, 09:00 - 10:00, Lecture hall EI 7

Abstract

As they allow processes to communicate and synchronize, concurrent objects are, de facto, the most important objects of concurrent programming. The talk will present and illustrate two important notions associated with such objects. The first one, which is related to their implementation, is the notion of a hybrid implementation. The second one, which is related to their definition, is the notion of an abortable object. Roughly speaking, a hybrid implementation of a concurrent object is such that the algorithms implementing its operations do not use locks in "good circumstances", those being defined statically or dynamically. In particular the use of locks must be prevented in concurrency-free execution patterns.

The notion of an abortable object is related to the object definition itself. It addresses the case where, in practice, conflicts are rare. So the idea is here to allow a process that invokes an object operation, to return a predefined default value (abort) in specific circumstances, namely in the presence of concurrency. To illustrate this, the talk will present a non-blocking implementation of an abortable stack (non-blocking means here that, in the presence of concurrency, at least one stack operation does not return abort).

Biography

Michel Raynal is a Professor of computing science, IRISA, University of Rennes, France. His main research interests are the basic principles of distributed computing systems. He is a world leading researcher in distributed computing, and the author of numerous papers on this topic (more than 140 in int'l scientific journals, more than 300 papers in int'l conferences). He is also well-known for his books on distributed computing.
Michel Raynal chaired the program committee of the major conferences on the topic (e.g., ICDCS, DISC, SIROCCO, OPODIS, ICDCN, etc.) and served on the program committees of more than 180 int'l conferences including all the most prestigious ones. He is the recipient of several "Best Paper" awards (including ICDCS 1999, 2000 and 2001, SSS 2009 and 2011, Europar 2010, DISC 2010, PODC

Keynotes

Keynote 2

2014) and has supervised more than 45 PhD students. He is also the winner of the 2015 Int'l Award "Innovation in Disitributed Computing" (also known as SIROCCO Prize). He gave lectures on distributed computing in many universities all over the world. In the recent past, Michel Raynal has written four books: "Communication and Agreement Abstractions for Fault-Tolerant Asynchronous Distributed Systems", Morgan & Claypool 251 pages, 2010 (ISBN 978-1-60845-293-4); "Fault-Tolerant Agreement in Synchronous Distributed Systems", 165 pages, Morgan & Claypool, September 2010), (ISBN 978-1-60845-525-6); "Concurrent Programming: Algorithms, Principles and Foundations", Springer, 515 pages, 2012 (ISBN 978-3-642-32026-2), and "Distributed Algorithms for Message-passing Systems", Springer, 510 pages, 2013 (ISBN: 978-3-642-32026-2). Since 2010, Michel Raynal is a senior member of the prestigious "Institut Universitaire de France".

Mateo Valero

Barcelona Supercomputing Centre, Spain

Runtime Aware Architectures

Thursday, Aug 27, 2015, 09:00 - 10:00, Lecture hall EI 7

Abstract

In the last few years, the traditional ways to keep the increase of hardware performance to the rate predicted by the Moore's Law have vanished. When unicores were the norm, hardware design was decoupled from the software stack thanks to a well defined Instruction Set Architecture (ISA). This simple interface allowed developing applications without worrying too much about the underlying hardware, while hardware designers were able to aggressively exploit instruction-level parallelism (ILP) in superscalar processors. With the irruption of multi-cores and parallel applications, this simple interface started to leak. As a consequence, the role of decoupling again applications from the hardware was moved to the runtime system. Efficiently using the underlying hardware from this runtime without exposing its complexities to the application has been the target of very active and prolific research in the last years. Current multi-cores are designed as simple symmetric multiprocessors (SMP) on a chip. However, we believe that this is not enough to overcome all the problems that multi-cores already have to face. It is our position that the runtime has to drive the design of future multi-cores to overcome the restrictions in terms of power, memory, programmability and resilience that multi-cores have. In this talk, we introduce a first approach towards a Runtime-Aware Architecture (RAA), a massively parallel architecture designed from the runtime's perspective.

Keynotes

Keynote 2

Biography

Mateo Valero is professor at the Computer Architecture Department at UPC, in Barcelona. His research interests focuses on high performance architectures. He has published approximately 600 papers, has served in the organization of more than 300 International Conferences and he has given more than 400 invited talks. He is the director of the Barcelona Supercomputing Centre, the National Centre of Supercomputing in Spain.

Dr. Valero has been honoured with several awards. Among them, the Eckert-Mauchly Award, Harry Goode Award, The ACM Distinguish Service award, the "King Jaime I" in research and two Spanish National Awards on Informatics and on Engineering. He has been named Honorary Doctor by the Universities of Chalmers, Belgrade and Veracruz in Mexico and by the Spanish Universities of Las Palmas de Gran Canaria, Zaragoza and Complutense in Madrid . "Hall of the Fame" member of the IST European Program (selected as one of the 25 most influents European researchers in IT during the period 1983-2008. Lyon, November 2008).

Professor Valero is Academic member of the Royal Spanish Academy of Engineering, of the Royal Spanish Academy of Doctors, of the Academia Europaea, and of the Academy of Sciences in Mexico, and Correspondant Academic of the Spanish Royal Academy of Science, He is a Fellow of the IEEE, Fellow of the ACM and an Intel Distinguished Research Fellow.

Keynotes

Keynote 3

Christian Scheideler

Universität Paderborn, Germany

Self-stabilizing distributed data structures

Friday, Aug 28, 2015, 11:00 - 12:00, Lecture hall EI 7

Abstract

Once a distributed system becomes large enough, faults are not the exception but the rule. Proactive strategies that aim at protecting a distributed system from becoming corrupted can only protect a system up to a certain point, which is nicely demonstrated by the CAP-Theorem and other impossibility results. So also reactive strategies, which aim at recovering from corruptions, should be considered. A standard approach to obtain systems that are able to recover from any kind of faults is self-stabilization. However, previous research has mostly focused on the case that there are no more faults or other changes to the system (due to pending requests) during self-stabilization. So it is not clear for many of the proposed solutions how well the system would be able to serve requests while it is self-stabilizing. In my presentation I will address this issue for the specific case of self-stabilizing distributed data structures that are managed by a large distributed system that does not just allow changes to the data but also to the set of its members, and I will present our newest results in this area.

Biography

Christian Scheideler received his M.S. and Ph.D. degrees in computer science from the University of Paderborn, Germany, in 1993 and 1996. After that, he was a postdoc at the Weizmann Institute, Israel, for a year, and a postdoc at the University of Paderborn, Germany, for two and a half years, which ended with his Habilitation in June 2000. From 2000 to 2005 he was an Assistant Professor (with tenure track) at the Johns Hopkins University, USA, and from 2005 to 2009 he was an Associate Professor at the Technical University of Munich, Germany. Since 2009 he is a Professor in the Department of Computer Science, University of Paderborn, and since October 2013 he is also the department chair. Christian Scheideler is (co)author of more than 100 publications in refereed conferences and journals and has served on more than 60 conference committees. He was a PC chair of DCOSS 2007 (algorithms track), SPAA 2007, IPDPS 2009 (algorithms track), Algosensors 2010, SSS 2012, SSS 2013 (P2P track), and SIROCCO 2015 and the general chair of SSS 2014. He was also a local arrangements chair of STOC 2005, SPAA 2008, and INFORMATIK 2008, and he has been the SPAA secretary since 2004.

The Future of Parallel, Distributed and High-Performance Computing, in Europe

16:00 - 17:30, Lecture hall EI 7

Panelists

Raffaele Tripiccione (Moderator)	University of Ferrara & INFN
Piero Altoe	E4 Computer Engineering
Wolfgang Nagel	ZIH & TU Dresden
Keshav Pingali	University of Texas, Austin
Michel Raynal	IRISA, University of Rennes

Abstract

We will discuss the state-of-affairs in parallel, distributed, and high performance computing, from both a technical/scientific and a political perspective, emphatically with a Euro-centric point of view. We encourage strong personal opinions and look forward to a lively discussion.

Topics that may be addressed are the following:

- Is parallel and distributed computing (still?) a relevant technical/scientific discipline? What are major open, scientific, and technical challenges? Are these being adequately tackled in Europe? If not, why not?
- European high-performance computing infrastructure - how, where?
- How does Europe compare to USA, China, Japan in HPC/parallel and distributed computing in terms of HPC infrastructure and scientific impact? Are we losing ground or catching up? What should, can, and must be done?
- European industry expectations and requirements, what are they? Are they stimuli or obstacles? Is our research relevant for the industry? Should we be concerned?
- Is the European (including national, including public universities and research institutions) funding adequate? Are the applied funding schemes and instruments conducive to high-quality research in parallel and distributed computing? Are research results efficiently transferred to industry?

Conference Program

Overview

Tuesday, Aug 25, 2015

19:00	Welcome Reception

Day 1 - Wednesday, Aug 26, 2015

08:45 - 09:00	Welcome Session, Opening Remarks		
09:00 - 10:00	Keynote 1		
10:00 - 10:30	Coffee Break		
10:30 - 12:00	Session 1A Topic 3	Session 1B Topic 13	Session 1C Topic 2
12:00 - 13:30	Lunch Break		
13:30 - 15:30	Session 2A Topic 3	Session 2B Topic 13	Session 2C Topic 5, Topic 6
15:30 - 16:00	Coffee Break		
16:00 - 18:00	Session 3A Topic 12, Topic 7	Session 3B Topic 1, Topic 8	Session 3C Topic 4

Day 2 - Thursday, Aug 27, 2015

09:00 - 10:00	Keynote 2	
10:00 - 10:30	Coffee Break	
10:30 - 12:00	Session 4: Distinguished Papers	
12:00 - 13:30	Lunch Break	
13:30 - 15:30	Session 5A Topic 3	Session 5B, Topic 9, Topic 13
15:30 - 16:00	Coffee Break	
16:00 - 17:30	Panel	
	Conference Banquet	

Day 3 - Friday, Aug 28, 2015

09:00 - 10:30	Session 6A Topic 10	Session 6B Topic 9	Session 6C Topic 12
10:30 - 11:00	Coffee Break		
11:00 - 12:30	Keynote 3, Euro-Par 2016 Preview, Closing Session		

Conference Program

Overview

The following topics will be covered by regular Euro-Par 2015 sessions:

Topic	Name	Sessions	Date	Slot
Topic 1	Support Tools and Environments	3B	Wednesday, Aug 26	16:00 - 18:00
Topic 2	Performance Modeling, Prediction and Evaluation	1C	Wednesday, Aug 26	10:30 - 12:00
Topic 3	Scheduling and Load Balancing	1A	Wednesday, Aug 26	10:30 - 12:00
		2A		13:30 - 15:30
		5A	Thursday, Aug 27	13:30 - 15:30
Topic 4	Architecture and Compilers	3C	Wednesday, Aug 26	16:00 - 18:00
Topic 5	Parallel and Distributed Data Management	2C	Wednesday, Aug 26	13:30 - 15:30
Topic 6	Grid, Cluster and Cloud Computing	2C	Wednesday, Aug 26	13:30 - 15:30
Topic 7	Distributed Systems and Algorithms	3A	Wednesday, Aug 26	16:00 - 18:00
Topic 8	Parallel and Distributed Programming, Interfaces and Languages	3B	Wednesday, Aug 26	16:00 - 18:00
Topic 9	Multicore and Manycore Programming	6B	Thursday, Aug 27	13:30 - 15:30
		5B	Friday, Aug 28	09:00 - 10:30
Topic 10	Theory and Algorithms for Parallel Computation	6A	Friday, Aug 28	09:00 - 10:30
Topic 12	Numerical Methods and Applications	6C	Wednesday, Aug 26	16:00 - 18:00
		3A	Friday, Aug 28	09:00 - 10:30
Topic 13	Accelerator Computing	1B	Wednesday, Aug 26	10:30 - 12:00
		2B		13:30 - 15:30
		5B	Thursday, Aug 27	13:30 - 15:30

Conference Program

Day 1 - Wednesday, Aug 26, 2015

Session 1A (Lecture hall EI 7), 10:30 - 12:00

T3: Scheduling and Load Balancing
Chair: Rizos Sakellariou

Concurrent Priority Queues are not Good Priority Schedulers
Andrew Lenharth, Donald Nguyen and Keshav Pingali

Load Balancing Prioritized Tasks via Work-Stealing
Shams Imam and Vivek Sarkar

Moody Scheduling for Speculative Parallelization
Alvaro Estebanez, Diego R. Llanos, David Orden and Belen Palop

Session 1B (Lecture hall EI 9), 10:30 - 12:00

T13: Accelerator Computing
Chair: Jens Breitbart

Effective Barrier Synchronization on Intel Xeon Phi Coprocessor
Andrey Rodchenko, Andy Nisbet, Antoniu Pop and Mikel Lujan

High-Performance and Scalable Design of MPI-3 RMA on Xeon Phi Clusters
Mingzhe Li, Khaled Hamidouche, Xiaoyi Lu, Jian Lin and Dhabaleswar Panda

Iterative Sparse Triangular Solves for Preconditioning
Hartwig Anzt, Edmond Chow and Jack Dongarra

Session 1C (Lecture hall EI 10), 10:30 - 12:00

T2: Performance Modeling, Prediction and Evaluation
Chair: Felix Wolf

Online Automated Reliability Classification of Queueing Models for Streaming Processing using Support Vector Machines
Jonathan Beard, Cooper Epstein and Roger Chamberlain

Low-overhead detection of memory access patterns and their time evolution
Harald Servat, German Llort, Juan Gonzalez Garcia, Judit Giménez and Jesús Labarta

Automatic On-line Detection of MPI Application Structure with Event Flow Graphs
Xavier Aguilar, Karl Fuerlinger and Erwin Laure

Session 2A (Lecture hall EI 7), 13:30 - 15:30

T3: Scheduling and Load Balancing
Chair: Olivier Beaumont

Locality and Balance for Communication-Aware Thread Mapping in Multicore Systems
Matthias Diener, Eduardo Cruz, Marco Antonio Zanata Alves, Mohammad Alhakeem, Philippe Navaux and Hans-Ulrich Heiss

Hardware Round-Robin Scheduler for Single-ISA Asymmetric Multi-Core
Nikola Markovic, Daniel Nemirovsky, Veljko Milutinovic, Osman Unsal, Mateo Valero and Adrian Cristal

A Multi-Level Hypergraph Partitioning Algorithm using Rough Set Clustering
Foad Lotfifar and Matthew Johnson

A Duplicate-Free State-Space Model for Optimal Task Scheduling
Michael Orr and Oliver Sinnen

Session 2B (Lecture hall EI 9), 13:30 - 15:30

T13: Accelerator Computing
Chair: Roger Chamberlain

High Performance Multi-GPU SpMV for Multi-component PDE-based Applications
Ahmad Abdelfattah, Hatem Ltaief and David Keyes

Improving Performance of Convolutional Neural Networks by Separable Filters on GPU
Hao-Ping Kang and Che-Rung Lee

Systematic Fusion of CUDA Kernels for Iterative Sparse Linear System Solvers
Jose I. Aliaga, Joaquin Pérez and Enrique S. Quintana-Orti

Efficient Execution of Multiple CUDA Applications using Transparent Suspend, Resume and Migration
Taichiro Suzuki, Akira Nukada and Satoshi Matsuoka

Session 2C (Lecture hall EI 10), 13:30 - 15:30

T5: Parallel and Distributed Data Management
T6: Grid, Cluster and Cloud Computing
Chair: Frédéric Desprez

Performance impacts with Reliable Parallel File Systems at Exascale level
Ramon Nou, Alberto Miranda and Toni Cortes

Rapid Tomographic Image Reconstruction via Large-Scale Parallelization
Tekin Bicer, Doga Gursoy, Rajkumar Kettimuthu, Francesco De Carlo, Gagan Agrawal and Ian T. Foster

VMPlaceS A Generic Tool to Investigate and Compare VM Placement Algorithms
Adrien Lèbre, Jonathan Pastor and Mario Südholt

Software consolidation as an efficient energy and cost saving solution for a SaaS/PaaS cloud model
Alain Tchana, Noel de Palma, Ibrahim Safieddine and Daniel Hagimont

Conference Program

Day 1 - Wednesday, Aug 26, 2015

Session 3A (Lecture hall EI 7), 16:00 - 18:00

T7: Distributed Systems and Algorithms
T12: Numerical Methods and Applications
Chair: Marian Vajteršic

DFEP: Distributed Funding-based Edge Partitioning
Alessio Guerrieri and Alberto Montresor

A Connectivity Model for Agreement in Dynamic Systems
Carlos Gómez-Calzado, Arnaud Casteigts, Alberto Lafuente and Mikel Larrea

Behavioral Non-Portability in Scientific Numeric Computing
Yijia Gu, Thomas Wahl, Mahsa Bayati and Miriam Leeser

Exploiting Task-Based Parallelism in Bayesian Uncertainty Quantification
Panagiotis Hadjidoukas, Panagiotis Angelikopoulos, Lina Kulakova, Costas Papadimitriou and Petros Koumoutsakos

Session 3B (Lecture hall EI 9), 16:00 - 18:00

T1: Support Tools and Environments
T8: Parallel and Distributed Programming, Interfaces and Languages
Chair: Karl Fuerlinger

PR-STM: Priority Rule Based Software Transactions on the GPU
Qi Shen, Craig Sharp, William Blewitt, Gary Ushaw and Graham Morgan

Leveraging MPI-3 Shared-Memory Extensions for Efficient PGAS Runtime Systems
Huan Zhou, Kamran Idrees and José Gracia

Event-Action Mappings for Parallel Tools Infrastructures
Tobias Hilbrich, Martin Schulz, Holger Brunst, Joachim Protze, Bronis R. de Supinski and Matthias S. Mueller

MPI Thread-level Checking for MPI+OpenMP Applications
Emmanuelle Saillard, Patrick Carribault and Denis Barthou

Session 3C (Lecture hall EI 10), 16:00 - 18:00

T4: Architecture and Compilers
Chair: Michael Philippsen

Optimizing Task Parallelism with Library-Semantics-Aware Compilation
Peter Thoman, Stefan Moosbrugger and Thomas Fahringer

Automatic Data Layout Optimizations for GPUs
Klaus Kofler, Biagio Cosenza and Thomas Fahringer

Data Layout Optimization for Portable Performance
Kamal Sharma, Ian Karlin, Jeff Keasler, James McGraw and Vivek Sarkar

Conference Program

Day 2 - Thursday, Aug 27, 2015

Session 4: Distinguished Papers (Lecture hall EI 7), 10:30 - 12:00

Chair: Martin Schulz

Fast Parallel Suffix Array on the GPU
Leyuan Wang, Sean Baxter and John Owens

A Practical Transactional Memory Interface
Shahar Timnat, Maurice Herlihy and Erez Petrank

Session 5A (Lecture hall EI 7), 13:30 - 15:30

T3: Scheduling and Load Balancing
Chair: Denis Trystram

On the Heterogeneity Bias of Cost Matrices when Assessing Scheduling Algorithms
Louis-Claude Canon and Laurent Philippe

Allocating jobs with periodic demands
Olivier Beaumont, Ikbel Belaid, Lionel Eyraud-Dubois and Juan-Angel Lorenzo-Del-Castillo

Non-preemptive Throughput Maximization for Speed-Scaling with Power-Down
Eric Angel, Evripidis Bampis, Vincent Chau and Kim Thang Nguyen

Scheduling tasks from selfish multi-tasks agents
Johanne Cohen and Fanny Pascual

Session 5B (Lecture hall EI 9), 13:30 - 15:30

T9: Multicore and Manycore Programming
T13: Accelerator Computing
Chair: Siegfried Benkner

Targeting the Parallella
Spiros N. Agathos, Alexandros Papadogiannakis and Vassilios V. Dimakopoulos

Accelerating Lattice Boltzmann Applications with OpenACC
Enrico Calore, Jiri Kraus, Sebastiano F. Schifano and Raffaele Tripiccione

A Multicore Parallelization of Continuous Skyline Queries on Data Streams
Tiziano De Matteis, Salvatore Di Girolamo and Gabriele Mencagli

A Fast and Scalable Graph Coloring Algorithm for Multi-core and Many-core Architectures
Georgios Rokos, Gerard Gorman and Paul Kelly

Conference Program

Day 3 - Friday, Aug 28, 2015

Session 6A (Lecture hall EI 7), 09:00 - 10:30

T10: Theory and Algorithms for Parallel Computation
Chair: Robert Elsässer

Efficient Nested Dissection for Multicore Architectures
Dominique Lasalle and George Karypis

Scheduling Trees of Malleable Tasks for Sparse Linear Algebra
Abdou Guermouche, Loris Marchal, Bertrand Simon and Frédéric Vivien

Elastic Tasks: Unifying Task Parallelism and SPMD Parallelism with an Adaptive Runtime
Alina Sbirlea, Kunal Agrawal and Vivek Sarkar

Session 6B (Lecture hall EI 9), 09:00 - 10:30

T9: Multicore and Manycore Programming
Chair: Thomas Fahringer

Scalable Data-driven PageRank: Algorithms, System Issues & Lessons Learned
Joyce Whang, Andrew Lenharth and Inderjit Dhillon

A Composable Deadlock-free Approach to Object-based Isolation
Shams Imam, Jisheng Zhao and Vivek Sarkar

How Many Threads Will Be Too Many? On the Scalability of OpenMP Implementations
Christian Iwainsky, Sergei Shudler, Alexandru Calotoiu, Alexandre Strube, Michael Knobloch, Christian Bischof and Felix Wolf

Session 6C (Lecture hall EI 10), 09:00 - 10:30

T12: Numerical Methods and Applications
Chair: Wilfried Gansterer

Semi-Discrete Matrix-Free Formulation of 3D Elastic Full Waveform Inversion Modeling
Stephen Moore, Devi Sudheer Chunduri, Sergiy Zhuk, Tigran Tchrakian, Ewout van den Berg, Albert Akhriev, Alberto Costa Nogueira Junior, Andrew Rawlinson and Lior Horesh

10,000 performance models per minute - scalability of the UG4 simulation framework
Andreas Vogel, Alexandru Calotoiu, Alexandre Strube, Sebastian Reiter, Arne Nägel, Felix Wolf and Gabriel Wittum

Parallelization of an advection-diffusion problem arising in edge plasma physics using hybrid MPI/OpenMP programming
Matthieu Kuhn, Guillaume Latu, Nicolas Crouseilles and Stéphane Genaud

Workshops

Overview

Monday, Aug 24, 2015

BigDataCloud - Big Data Management in Clouds	Room EI 5
Euro-EDUPAR - Parallel and Distributed Computing Education for Undergraduate Students	Room EI 3
LSDVE - Large Scale Distributed Virtual Environments	Room EI 1
OMHI - On-chip Memory Hierarchies and Interconnects: organization, management and implementation	Room EI 3A
PADABS - Parallel and Distributed Agent-Based Simulations	Room EI 4
Resilience - Resiliency in High Performance Computing with Clouds, Grids, and Clusters	Room EI 2

Tuesday, Aug 25, 2015

HeteroPar - Algorithms, Models, and Tools for Parallel Computing on Heterogeneous Platforms	Room EI 3
PELGA - Performance Engineering for Large-scale Graph Analytics	Room EI 1
REPPAR - Reproducibility in Parallel Computing	Room EI 5
ROME - Runtime and Operating Systems for the Many-core Era	Room EI 4
UCHPC - UnConventional High Performance Computing	Room EI 2
VHPC - Virtualization in High-Performance Cloud Computing	Room EI 3A

Workshops

Overview

Monday, Aug 24, 2015

Time/Room	E1	EI 2	EI 3	EI 3A	EI 4	EI 5
09:00 - 10:30		Resilience	Euro-EDUPAR	OMHI	PADABS	BigData Cloud
10:30 - 11:00	Coffee Break					
11:00 - 12:30		Resilience	Euro-EDUPAR	OMHI	PADABS	BigData Cloud
12:30 - 14:00	Lunch Break					
14:00 - 16:00	LSDVE	Resilience	Euro-EDUPAR		PADABS	
16:00 - 16:30	Coffee Break					
16:30 - 18:00	LSDVE	Resilience	Euro-EDUPAR		PADABS	

Tuesday, Aug 25, 2015

Time/Room	EI 1	EI 2	EI 3	EI 3A	EI 4	EI 5
09:00 - 10:30	PELGA		HeteroPar	VHPC	ROME	REPPAR
10:30 - 11:00	Coffee Break					
11:00 - 12:30	PELGA		HeteroPar	VHPC	ROME	REPPAR
12:30 - 14:00	Lunch Break					
14:00 - 16:00	PELGA	UCHPC	HeteroPar			REPPAR
16:00 - 16:30	Coffee Break					
16:30 - 18:00	PELGA	UCHPC	HeteroPar			REPPAR
19:00	Welcome Reception					

Workshops Program

Monday, Aug 24, 2015

BigDataCloud - Big Data Management in Clouds

Room EI 5

Chairs: Alexandru Costan, Frédéric Desprez

Session 1

Monday, Aug 24, 2015, 09:00 - 10:30
Chair: Frédéric Desprez (Inria / LIP ENS Lyon)
Workshop Introduction

Distributed Range-Based Meta-Data Management for an In-Memory Storage
Florian Klein, Kevin Beineke, Michael Schöttner

File-less Approach to Large Scale Data Management
Bartosz Kryza, Jacek Kitowski

Session 2

Monday, Aug 24, 2015, 11:00 - 12:30
Chair: Alexandru Costan (IRISA / INSA Rennes)
Keynote
TBA

Network-based Data Processing Architecture for Reliable and High-performance Distributed Storage System
Hiroki Ohtsuji, Osamu Tatebe

Euro-EDUPAR - Parallel and Distributed Computing Education for Undergraduate Students

Room EI 3

Chairs: Sushil K. Prasad, Arnold L. Rosenberg, Domingo Giménez

Session 1

Monday, Aug 24, 2015, 09:00 - 10:30
Opening remarks
Arnold L. Rosenberg

Keynote presentation - Challenges of a Systematic Approach to Parallel Computing and Supercomputing Education
Vladimir Voevodin, Victor Gergel and Nina Popova

Position paper - Parallelism vs Distributed Computing: a Great Confusion?
Michel Raynal

Workshops Program

Monday, Aug 24, 2015

Session 2: Parallelism in Sciences and Engineering

Monday, Aug 24, 2015, 11:00 - 12:30

Teamwork Across Disciplines: High-Performance Computing Meets Engineering
Philipp Neumann, Christoph Kowitz, Felix Schranner and Dmitrii Azarnykh

Teaching Parallel Programming in Interdisciplinary Studies
Eduardo Cesar, Ana Cortés, Antonio Espinosa, Tomas Margalef, Anna Sikora, Remo Suppi and Juan Carlos Moure

Teaching Heart Modeling and Simulation on Parallel Computing Systems
Andrey Sozykin, Mikhail Chernoskutov, Anton Koshelev, Vladimir Zverev, Konstantin Ushenin and Olga Solovyova

Interdisciplinary practical course on parallel finite element method using HiFlow3
Markus Hoffmann, Eva Treiber, Simon Gawlok, Wolfgang Karl and Vincent Heuveline

Session 3: Courses and experiences

Monday, Aug 24, 2015, 14:00 - 16:00

Concurrent and Parallel Interactive Theoretical Teaching through ICT
Antonio J. Tomeu-Hardasmal, Alberto Salguero and Manuel I. Capel Tuñón

An Educational Module Illustrating how Sparse Matrix-Vector Multiplication on Parallel Processors Connects to Graph Partitioning
M. Ali Rostami and Martin Buecker

Panel: Parallel and Distributed Computing Teaching in Europe, necessities and perspectives
Henri E. Bal (Vrije Universiteit Amsterdam), Arnold L. Rosenberg (Northeastern Univ., Boston), Rizos Sakellariou (University of Manchester), Denis Trystram (Grenoble Institute of Technology), Vladimir Voevodin (Moscow State University)

Session 4: Tools for Teaching Parallelism

Monday, Aug 24, 2015, 16:30 - 18:00

SAUCE: A Web-based Automated Assessment Tool for Teaching Parallel Programming
Moritz Schlarb, Christian Hundt and Bertil Schmidt

FerbJmon Tools - Visualizing Thread Access on Java Objects using Light-weight Runtime Monitoring
Marvin Ferber

On line service for teaching parallel programming
Marek Nowicki, Maciej Marchwiany, Maciej Szpindler and Piotr Bala

Closing remarks

Workshops Program

Monday, Aug 24, 2015

LSDVE - Large Scale Distributed Virtual Environments

Room EI 1

Chairs: Laura Ricci, Alexandru Iosup, Radu Prodan

Session 1

Monday, Aug 24, 2015, 14:00 - 16:00

Workshop introduction
Laura Ricci

Offloading service provisioning on mobile devices in mobile computing environments
Marco Conti, Davide Mascitti and Andrea Passarella

Community Discovery for Interest Management in DVEs: a case Study
Emanuele Carlini, Patrizio Dazzi, Matteo Mordacchini, Alessandro Lulli and Laura Ricci

Session 2

Monday, Aug 24, 2015, 16:30 - 18:00

A Systematic Quality Analysis of Virtual Desktop Infrastructures Technologies
Arman Sheikholeslami and Kalman Graffi

Continuation Complexity: A Callback Hell for Distributed Systems
Edgar Zamora-Gómez, Pedro García-López and Rubén Mondéjar

A Trustworthy Distributed Social Carpool Method
Francisco Martin-Fernandez, Pino Caballero-Gil and Cándido Caballero-Gil

Concluding Remarks and Workshop Closing

OMHI - On-chip Memory Hierarchies and Interconnects: organization, management and implementation

Room EI 3A

Chairs: Julio Sahuquillo, Maria Engracia Gómez, Salvador Petit

Session 1

Monday, Aug 24, 2015, 09:00 - 10:30

Welcome and Opening Remarks

Keynote: Illuminating processors: how photonics will help computing
Sandro Bartolini

Workshops Program

Monday, Aug 24, 2015

Session 2

Monday, Aug 24, 2015, 11:00 - 12:30

Efficient DVFS Operation in NoCs through a Proper Congestion Management Strategy
Jose Vicente Escamilla Lopez, Jose Flich and Pedro Javier Garcia

Superoptimizing Memory Subsystems for Multiple Objectives
Joseph Wingbermuehle, Ron Cytron and Roger Chamberlain

PADABS - Parallel and Distributed Agent-Based Simulations

Room EI 4

Chairs: Vittorio Scarano, Gennaro Cordasco, Ugo Erra, Carmine Spagnuolo

Session 1: Welcome to PADABS

Monday, Aug 24, 2015, 09:00 - 10:30

Chair: Paul Richmond

Welcome
Vittorio Scarano, Gennaro Cordasco and Ugo Erra

Panel 'Distributed Open Agent-Based Simulation Benchmark'

Session 2: Load Balancing on Agent-Based Simulations

Monday, Aug 24, 2015, 11:00 - 12:30

Chair: Vittorio Scarano

Large-Scale Agent-based Modeling with Repast HPC: A Case Study in Parallelizing an Agent-based Model
Nick Collier, Jonathan Ozik and Charles Macal

On Evaluating Graph Partitioning Algorithms for Distributed Agent Based Models on Networks
Alessia Antelmi, Gennaro Cordasco, Carmine Spagnuolo and Luca Vicidomini

Graph-Based Automatic Dynamic Load Balancing for HPC Agent-Based Simulations
Claudio Márquez, Eduardo Cesar and Joan Sorribes

Session 3: Parallel and Distributed Agent-Based Simulations

Monday, Aug 24, 2015, 14:00 - 16:00
Chair: Carmine Spagnuolo

Behavioral Spherical Harmonics for Long-Range Agents' Interaction
Biagio Cosenza

Road Network Simulation using FLAME GPU
Peter Heywood, Paul Richmond and Steve Maddock

A communication schema for parallel and distributed Multi-Agent Systems based on MPI
Alban Rousset, Bénédicte Herrmann, Christophe Lang and Laurent Philippe

Session 4: Distributed Agent-Based Simulations and Practice

Monday, Aug 24, 2015, 16:30 - 18:00
Chair: Gennaro Cordasco

RAMSES: Reversibility-based Agent Modeling and Simulation Environment with Speculation-support
Davide Cingolani, Alessandro Pellegrini and Francesco Quaglia

Distributed Agent-based Simulation and GIS: An Experiment With the dynamics of Social Norms
Nicola Lettieri, Carmine Spagnuolo and Luca Vicidomini

Preliminary Evaluation of a Parallel Trace Replay Tool for HPC Network Simulations
Bilge Acun, Nikhil Jain, Abhinav Bhatele, Misbah Mubarak, Christopher D. Carothers and Laxmikant Kale

Resilience - Resiliency in High Performance Computing with Clouds, Grids, and Clusters

Room El 2

Chairs: Stephen L. Scott, Chokchai (Box) Leangsuksun

Session 1

Monday, Aug 24, 2015, 09:00 - 10:30

Opening
Stephen L. Scott

Keynote: Toward A Fault Model And Resilience Design Patterns For Extreme Scale Systems
Christian Engelmann

Workshops Program

Monday, Aug 24, 2015

Session 2

Monday, Aug 24, 2015, 11:00 - 12:30

A Holistic Approach To Log Data Analysis In High-Performance Computing Systems: The Case Of IBM Blue Gene/Q
Alina Sirbu and Ozalp Babaoglu

Canaries In A Coal Mine: Using Application-Level Checkpoints To Detect Memory Failures
Patrick Widener, Kurt Ferreira, Scott Levy and Nathan Fabian

A Case Study Of Application Structure Aware Resilience Through Differentiated State Saving And Recovery
Anshu Dubey, Hajime Fujita, Zachary Rubenstein, Brian Van Straalen and Andrew Chien

Session 3

Monday, Aug 24, 2015, 14:30 - 16:00

Addressing The Last Roadblock For Message Logging In HPC: Alleviating The Memory Requirement Using Dedicated Resources
Tatiana Martsinkevich, Thomas Ropars and Franck Cappello

Towards Understanding Post-Recovery Efficiency For Shrinking And Non-Shrinking Recovery
Aiman Fang, Hajime Fujita and Andrew Chien

An Advanced Fault-Tolerant Architecture For IP Routers
Waleed Aloriny and Chris Guy

Session 4

Monday, Aug 24, 2015, 16:30 - 18:00

Discussion: Future Directions For HPC Resilience Research

Closing
Stephen L. Scott

Workshops Program

Tuesday, Aug 25, 2015

HeteroPar - Algorithms, Models, and Tools for Parallel Computing on Heterogeneous Platforms

Room EI 3

Chair: Alexandru Iosup

Session 1

Tuesday, Aug 25, 2015, 09:00 - 10:30

Meet and Greet

Welcome Note

Keynote

Session 2

Tuesday, Aug 25, 2015, 11:00 - 12:30

A randomized LU-based solver using GPU and Intel Xeon Phi accelerators
Marc Baboulin, Amal Khabou and Adrien Remy

Towards Community Detection on Heterogenous Platforms
Stijn Heldens, Ana Lucia Varbanescu, Arnau Prat-Pérez and Josep-Lluis Larriba-Pey

Accelerating Direction-Optimized Breadth First Search on Hybrid Architectures
Scott Sallinen, Abdullah Gharaibeh and Matei Ripeanu

Session 3

Tuesday, Aug 25, 2015, 14:00 - 16:00

Communication models insights meet simulations
Pierre-Francois Dutot, Millian Poquet and Denis Trystram

Modeling Contention and Mapping Effects in Multi-core Clusters
Juan-Antonio Rico-Gallego, Juan-Carlos Díaz-Martín and Alexey L. Lastovetsky

Identifying Optimization Opportunities within Kernel Execution in GPU Codes
Robert Lim, Allen Malony, Boyana Norris and Nick Chaimov

FiNS: A Framework for Accelerating Nested Simulations on Heterogeneous Platforms
Joris Cramwinckel, Ana Lucia Varbanescu and Stefan Singor

Session 4

Tuesday, Aug 25, 2015, 16:30 - 18:00

A Design Proposal for a Next Generation Scientific Software Framework
Anshu Dubey and Daniel Graves

Panel: Next Generation Heterogeneous Computing

Workshops Program

Tuesday, Aug 25, 2015

PELGA - Performance Engineering for Large-scale Graph Analytics

Room EI 1

Chairs: Ana Lucia Varbanescu, Alexandru Iosup

Session 1

Tuesday, Aug 25, 2015, 09:00 - 10:30

Welcome Note

Invited Talk

Session 2

Tuesday, Aug 25, 2015, 11:00 - 12:30

Accelerating minimum spanning forest computations on multicore platforms
Guojing Cong

Quantifying the Performance Impact of Graph Structure on Neighbours Iteration Strategies
Merijn Verstraaten, Ana Lucia Varbanescu and Cees De Laat

Using the Marshall-Olkin Extended Zipf distribution in Graph Generation
Ariel Duarte López, Arnau Prat Pérez and Marta Pérez Casany

Session 3

Tuesday, Aug 25, 2015, 14:00 - 16:00

Invited Talk

Can Embedding Solve Scalability Issues for Mixed-Data Graph Clustering?
Nadezda Fedorova, Josep Blat and David Nettleton

A Multi-Layer Framework for Graph Processing via Overlay Composition
Alessandro Lulli, Patrizio Dazzi, Laura Ricci and Emanuele Carlini

Session 4

Tuesday, Aug 25, 2015, 16:30 - 18:00

Highspeed Graph Processing Exploiting Main-Memory Column Stores
Matthias Hauck, Marcus Paradies, Holger Fröning, Wolfgang Lehner and Hannes Rauhe

Characterizing Communication Patterns of Parallel Programs through Graph Visualization and Analysis
Denise Stringhini and Alvaro Fazenda

Importance of Runtime Considerations in Performance Engineering of Large-Scale Distributed Graph Algorithms
Jesun Sahariar Firoz, Thejaka Amila Kanewala, Marcin Zalewski, Martina Barnas and Andrew Lumsdaine

Closing Notes

Workshops Program

Tuesday, Aug 25, 2015

REPPAR - Reproducibility in Parallel Computing

Room EI 5

Chairs: Sascha Hunold, Arnaud Legrand, Lucas Nussbaum, Mark Stillwell

Session 1

Tuesday, Aug 25, 2015, 09:00 - 10:30

Workshop Introduction and Survey Announcement

Keynote 1: Realistic and Reproducible Wireless Networking Experiments
Walid Dabbous

Session 2

Tuesday, Aug 25, 2015, 11:00 - 12:30

Reproducible and User-Controlled Software Environments in HPC with Guix
Ludovic Courtès and Ricardo Wurmus

Reproducibility in Practice: Lessons learned from Research and Teaching Experiments
Antonio Maffia, Helmar Burkhart and Danilo Guerrera

Towards Complete Tracking of Provenance in Experimental Distributed Systems Research
Tomasz Buchert, Lucas Nussbaum and Jens Gustedt

Session 3

Tuesday, Aug 25, 2015, 14:00 - 16:00

Keynote 2: Some Obstacles on the Way to Reproducibility of Performance Measurements
Gerhard Wellein

Mini-Tutorials on Tools and Methods to Support Reproducible Research

- Effective Data Visualization/Presentation with R/ggplot2, *Arnaud Legrand*
- Testbeds for Reproducible Research, *Lucas Nussbaum*
- Data Analysis with Jupyter, *Mark Stillwell*
- Measurement Bias introduced by MPI_Barrier, *Sascha Hunold*

Session 4

Tuesday, Aug 25, 2015, 16:30 - 18:00

Survey Evaluation and Open Discussion on the State of Reproducibility in Parallel Computing and the Future of REPPAR

Workshops Program

Tuesday, Aug 25, 2015

ROME - Runtime and Operating Systems for the Many-core Era

Room EI 4

Chairs: Stefan Lankes, Carsten Clauss

Session 1

Tuesday, Aug 25, 2015, 09:00 - 10:30

Welcome speech and announcements

Invited talk: A Microkernel-based Operating System for Exascale Computing
Carsten Weinhold

Diamond Rings: Acknowledged Event Propagation in Many-Core Processors
Stefan Nürnberger, Randolf Rotta, Gabor Drescher, Daniel Danner and Jörg Nolte

Session 2

Tuesday, Aug 25, 2015, 11:00 - 12:30

An OS-oriented performance monitoring tool for multicore systems
Juan Carlos Saez, Jorge Casas, Abel Serrano, Roberto Rodríguez-Rodríguez, Fernando Castro, Daniel Chaver and Manuel Prieto-Matias

A Performance Analysis Tool for Parallel Application Placement on Hierarchical Architectures
Nicolas Denoyelle, Brice Goglin and Emmanuel Jeannot

Energy Characterization and Optimization of Parallel Prefix-Sums Kernels
Angelos Papatriantafyllou

UCHPC - UnConventional High Performance Computing

Room EI 2

Chairs: Jens Breitbart, Josef Weidendorfer

Session 1

Tuesday, Aug 25, 2015, 14:00 - 16:00

Chair: Jens Breitbart

Workshop opening
Josef Weidendorfer, Jens Breitbart

Keynote - The Active Memory Cube: A Processing-in-Memory System for High Performance Computing
Zehra Sura

Energy-performance tradeoffs for HPC applications on low power processors
Enrico Calore, Sebastiano Fabio Schifano, Raffaele Tripiccione

Session 1 (continued)

Optimized Force Calculation of Molecular Dynamics Simulations for the Intel Xeon Phi
Nikola Tchipev, Amer Wafai, Colin W. Glass, Wolfgang Eckhardt, Alexander Heinecke, Hans-Joachim Bungartz, Philipp Neumann

Session 2

Tuesday, Aug 25, 2015, 16:30 - 18:00
Chair: Josef Weidendorfer
Towards Application Variability Handling with Component Models: 3D-FFT Use Case Study
Jérôme Richard, Vincent Lanore, Christian Perez

A cache-aware performance prediction framework for GPGPU computations
Alexander Pöppl, Alexander Herz

Best Paper Award Ceremony and Workshop Closing
Josef Weidendorfer, Jens Breitbart

VHPC - Virtualization in High-Performance Cloud Computing

Room EI 3A

Chairs: Michael Alexander, Anastassios Nanos, Balazs Gerofi

Session 1

Tuesday, Aug 25, 2015, 09:00 - 10:30
Performance evaluation of containers for HPC
Cristian Ruiz, Emmanuel Jeanvoine and Lucas Nussbaum

A Simplified TDP with Lookup Tables
Yu Zhang

GPGPU Virtualization with multi-API support using Containers
John Walsh and Jonathan Dukes

Session 2

Tuesday, Aug 25, 2015, 11:00 - 12:30
The Virtual Puppet Master: adaptive streaming on top of an SDN-enabled virtual infrastructure
Simon Pietro Romano, Roberto Canonico, Enrico De Maio and Pasquale Di Rienzo

Invited Talk: The App Container Specification: Designing an open standard for running applications in containers
Jonathan Boulle

Closing remarks

Social Events

Welcome Reception

Venue: Vienna City Hall

The Euro-Par 2015 Welcome Reception will take place at the Vienna City Hall on Tuesday, August 25, 2015, starting from 19:30.

The city hall is easily reachable by public transportation from the conference site. The "Karlsplatz" subway station is located nearby the conference venue, and it provides a direct connection to the city hall: you can use the U2 line to get to the Rathaus station.

Additionally, the city hall is reachable by several tram lines, such as 1, D, 71 from the "Opernring" station.

Conference Banquet

Venue: Schottenheuriger, Liechtensteinstr. 68, A-2344 Maria Enzersdorf

The conference banquet will be held at a typical Viennese "Heuriger", the Schottenheuriger.

Buses will be available to take the participants to the banquet venue and back to the Vienna city center. Buses are scheduled to leave at 18:45.

Please do not forget to bring your conference badge and the ticket of accompanying persons, as they will be checked before getting on the buses.

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